TEXAS INSTRUMENTS

application INFO available

UC2886
UC3886

Average Current Mode PWM Controller IC

FEATURES

- 10.3V - 20V Operating Range
- Low Offset Voltage Amplifier
- High Bandwidth Current and Voltage Amplifiers
- Low Offset Current Sense Amplifier
- Undervoltage Lockout
- Trimmed 5 Volt Reference
- Externally Programmable Oscillator Charge Current
- 1.5A Peak Totem Pole Output
- Available in 16-pin DIL or SOIC Packages

DESCRIPTION

The UC3886 family of PWM controller ICs is designed for DC-to-DC converters with average current mode control. It is designed for use in conjunction with the UC3910 4-bit DAC and Voltage Monitor. The UC3886 drives an external N-channel MOSFET and can be used to power the Intel Pentium® Pro and other high-end microprocessors.

The UC3886 in conjunction with the UC3910 converts 5VDC to an adjustable output ranging from 2.0V to 3.5V in 100mV steps with 35mV DC system accuracy.

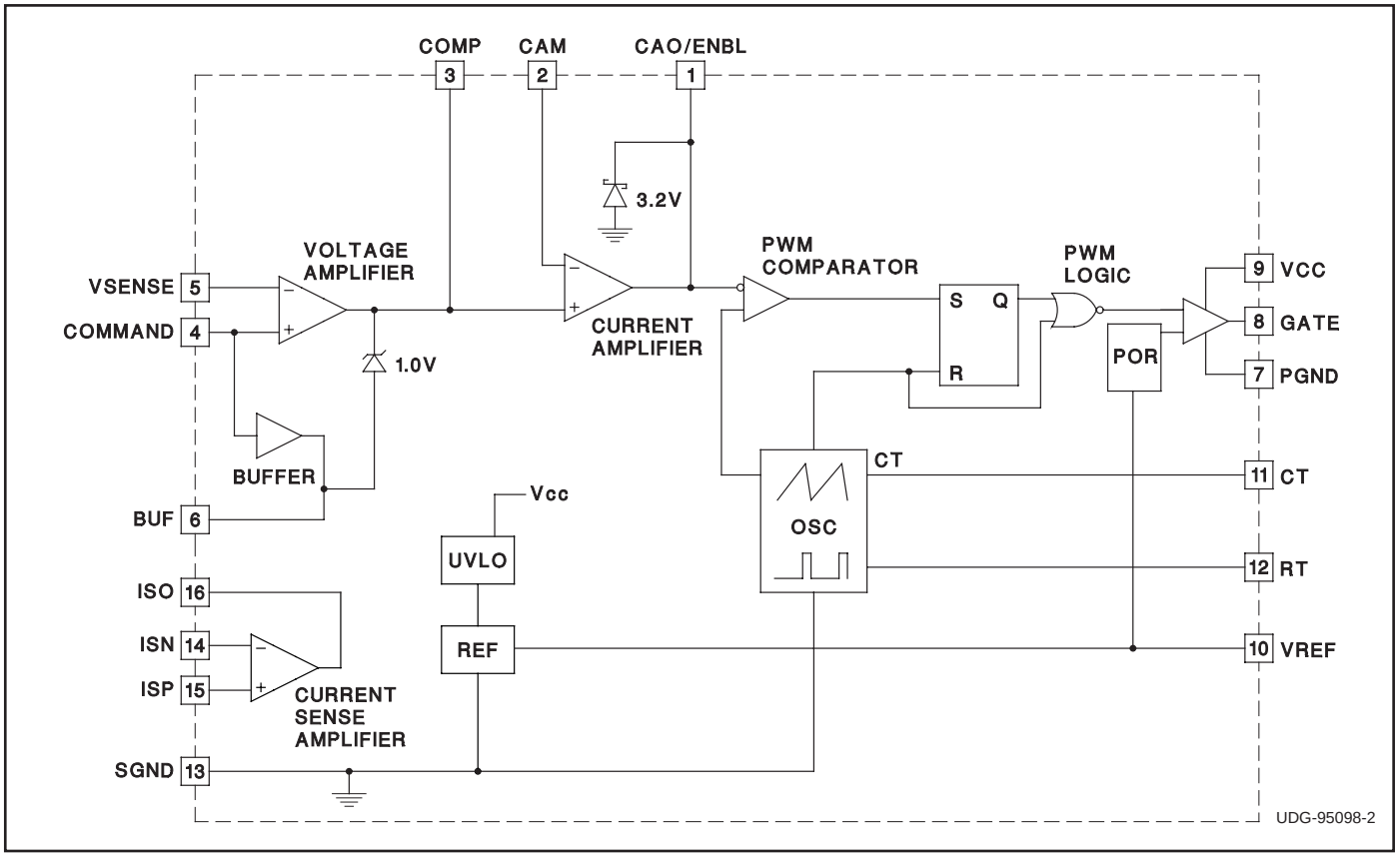
The oscillator is programmed by the user's selection of an external resistor and capacitor, and is designed for 300kHz typical operation.

The voltage and current amplifiers have 3.5MHz gain-bandwidth product to satisfy high performance system requirements.

The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. It has inputs and outputs accessible to allow user-selection of gain-setting resistors, and is internally compensated for a gain of 5 and above. The command voltage input is buffered and provided for use as the reference for the current sense amplifier.

The output of the voltage amplifier (input to the current amplifier) is clamped to 1 volt above the command voltage to serve as a current limit. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8 volts.

BLOCK DIAGRAM



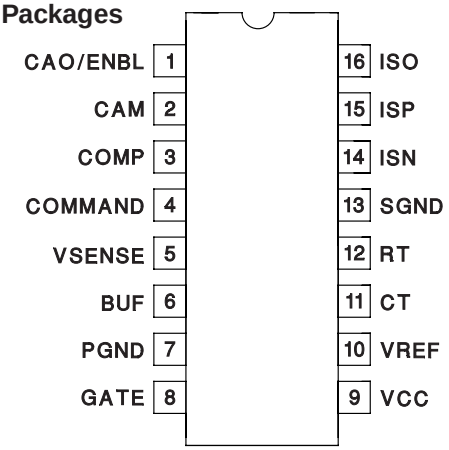
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Output Current
CAM, COMMAND, VSENSE, ISN, ISP . . . . . ± 1A
Analog Input . . . . . –0.3V to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperatue (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 12V, $V_{COMMAND}$ = 3.0V, CT = 1nF, RT = 10k, $T_A = T_J$ = 0°C < T_A < 70°C for the UC3886. (Note: –25°C < T_A < 85°C for the UC2886,

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current	VCC = 11V, Gate Open		10	15	mA
	VCC = 9.3V			5	mA
Undervoltage Lockout					
Start Threshold		9.7	10.3	10.8	V
UVLO Hysteresis			0.25	0.4	V
Voltage Error Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			4	mV
	V_{CM} = 3.0V (UC2886)			15	mV
Input Bias Current	V_{CM} = 3.0V			–2	µA
Input Offset Current	V_{CM} = 3.0V (UC3886)			0.01	µA
	V_{CM} = 3.0V (UC2886)			0.1	µA
Open Loop Gain	2.5V < V_{COMP} < 3.5V	60	85		dB
Common-Mode Rejection Ratio	2V < V_{COMP} < 4V	60	85		dB
Power Supply Rejection Ratio	11V < VCC < 15V	60	85		dB
Output High Voltage (Clamp)	I_{COMP} = –100µA (UC3886)	3.95	4	4.05	V
	I_{COMP} = –100µA (UC2886)	3.9		4.1	V
Output Low Voltage (Clamp)	I_{COMP} = 100µA	1.9		2.7	V
Output Sink Current	V_{COMP} = 3.7V	0.9			mA
Output Source Current	V_{COMP} = 2.8V	–0.15	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
5.0V Reference					
Output Voltage	I_{VREF} = 1.0mA	4.9	5	5.1	V
Total Variation	Line, Load, Temperature	4.825		5.175	V
Line Regulation	11V < VCC < 15V			10	mV
Load Regulation	0 < I_{VREF} < 2mA			15	mV
Short Circuit Current		–10		–40	mA

ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 12V, $V_{COMMAND}$ = 3.0V, CT = 1nF, RT = 10k, $T_A = T_J$ = 0°C < T_A < 70°C for the UC3886. (Note: –25°C < T_A < 85°C for the UC2886,

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Buffer					
Gain	I_{BUF} = ± 500µA (UC3886)	0.98	1	1.02	V/V
	I_{BUF} = ± 500µA (UC2886)	0.95		1.05	V/V
Current-Sense Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			2	mV
	V_{CM} = 3.0V (UC2886)			6	mV
Input Bias Current	V_{CM} = 3.0V			-1	µA
Input Offset Current	V_{CM} = 3.0V			0.2	µA
Open Loop Gain	2V < V_{ISO} < 6V	60	85		dB
CMRR	0V < V_{CM} < 4.5V	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{ISO} = –100µA	5			V
Output Low Voltage	I_{ISO} = 1mA			1	V
Output Source Current	V_{ISO} = 2V	–0.2			mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			13	mV
	V_{CM} = 3.0V (UC2886)			18	mV
Input Bias Current	V_{CM} = 3.0V			1	µA
Open Loop Gain	1V < V_{CAO} < 3V	60	85		dB
CMRR	1.5V < V_{CM} < 4.5V	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{CAO} = –100µA	3		3.3	V
Output Low Voltage	I_{CAO} = 100µA			1	V
Output Source Current	V_{CAO} =1V	–0.1	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Oscillator					
Frequency	RT = 10k, CT = 1nF (UC3886)	90	100	110	kHz
	RT = 10k, CT = 1nF (UC2886)	85		115	kHz
Frequency Change With Voltage	11V > VCC > 15V			1	%
CT Peak Voltage		2.6	2.8		V
CT Valley Voltage			1	1.2	V
CT Peak-to-Peak Voltage		1.6	1.8	2.0	V
Output Section					
Output Low Voltage	I_{GATE} = 200mA		1.6	2.2	V
Output High Voltage	I_{GATE} = –200mA	9	10.3		V
Output Low Voltage	5V < VCC < 9V, I_{GATE} = 10mA			0.5	V
	V_{CAO} < 0.8V, I_{GATE} = 10mA			0.5	V
Rise/Fall Time	C_L = 1nF			150	ns
Maximum Duty Cycle	(UC3886)	90			%
	(UC2886)	85			%

PIN DESCRIPTIONS

BUF: (Buffer Output) The voltage on COMMAND pin is buffered and presented to the user here. This voltage is used to provide the operating bias point for the current sense amplifier by connecting a resistor between BUF and ISP. Decouple BUF with 0.01µF or greater to SGND.

CAM: (Current Amplifier Minus Input) The average load current feedback from ISO is typically applied through a resistor here.

CAO/ENBL: (Current Amplifier Output/Chip Enable) The current loop compensation network is connected between CAO/ENBL and CAM, the inverting input of the current amplifier. The voltage at CAO/ENBL is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage at this pin exceeds 1.0 volts, allowing the PWM to force zero duty cycle when necessary. The user can force this pin below 0.8 volts externally with an open collector, disabling the GATE drive.

COMMAND: (Voltage Amplifier Non-Inverting Input) This input to the voltage amplifier is connected to a command voltage, such as the output of a DAC. This voltage sets the switching regulator output voltage.

COMP: (Compensation, Voltage Amplifier Output) The system voltage compensation network is applied between COMP and VSENSE. The voltage at COMP is clamped to prevent it from going more than 1V above the COMMAND voltage. This is used to provide an accurate average current limit. The voltage on COMP is also clamped to 0.7V below the voltage on COMMAND. This is done to avoid applying a full charge to capacitors in the compensation network during transients, allowing quick recovery time and little overshoot.

CT: (Oscillator Timing Capacitor) A capacitor from CT to SGND along with the resistor on RT, sets the PWM frequency and maximum duty cycle according to these formulas:

$$D_{MAX} = 1 - \frac{2.0V}{RT \bullet 4.0mA}$$

where D_{MAX} is the maximum operating duty cycle, and RT is in ohms.

$$F_{OSC} = \frac{2.0V \bullet \left(\left(4.0mA \bullet RT \right) - 2.0V \right)}{CT \bullet 1.8V \bullet RT^2 \bullet 4.0mA}$$

where F_{OSC} is the UC3886 oscillator switching frequency in Hz, RT is in ohms, and CT is in farads.

GATE: (PWM Output) The output is a 1A totem pole driver. Use a series resistor of at least 5 to prevent interaction between the gate impedance and the output driver that might cause excessive overshoot.

ISN: (Current Sense Amplifier Inverting Input) A resistor to the low side of the average current sense resistor and a resistor to ISO are applied to this pin to make a differential sensing amplifier.

ISO: (Current Sense Amplifier Output) A feedback resistor to ISN is connected here to make a differential sensing amplifier. The voltage at this pin is equal to (V_{BUF} + A • I_{AVG} • R_{SENSE}) where A is the user determined gain of the differential amplifier, I_{AVG} is the average load current of the system, and R_{SENSE} is the average current sensing resistor. For stability, A must be greater than 5. Set A such that A • I_{SC} • R_{SENSE} = 1.0V where ISC is the user-determined short circuit current limit.

ISP: (Current Sense Amplifier Non-Inverting Input) A resistor to the high side of the average current sense resistor and a resistor to BUF are connected to this pin to make a differential sensing amplifier.

PGND: (Power Ground) The PWM output current returns to ground through this pin. This is separated from SGND to avoid on-chip ground noise generated by the output current.

RT: (Oscillator Charging Current) This pin is held at 2V. Resistor RT from this pin to SGND sets the oscillator charging current. Use 5k < RT < 100k.

SGND: (Signal Ground) For better noise immunity, signal ground is provided at this pin.

VCC: (Positive Supply Voltage) This pin supplies power to the chip and to the gate drive output. Decouple to PGND and separately to SGND for best noise immunity. The reference (VREF), GATE output, oscillator, and amplifiers are disabled until VCC exceeds 10.3V.

VREF: (Voltage Reference Output) An accurate 5V reference as provided at this pin. The output can deliver 2mA to external circuitry, and is internally short circuit current limited. VREF is disabled if VCC is below UVLO. Bypass 5V REF to SGND with an 0.01µF or larger capacitor for best stability.

VSENSE: (Voltage Sense Input) This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

APPLICATION INFORMATION

OSCILLATOR

The UC3886 oscillator is a saw tooth. The rising edge is governed by a current controlled by RT flowing into the capacitor CT. The falling edge of the sawtooth sets the dead time for the output. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency, Fs, and the value of RT. The design equations are:

$$D_{MAX} = 1 - \frac{2.0V}{RT \bullet 4.0mA}$$

$$F_{OSC} = \frac{2.0V \bullet \left((4.0mA \bullet RT) - 2.0V \right)}{CT \bullet 1.8V \bullet RT^2 \bullet 4.0mA}$$

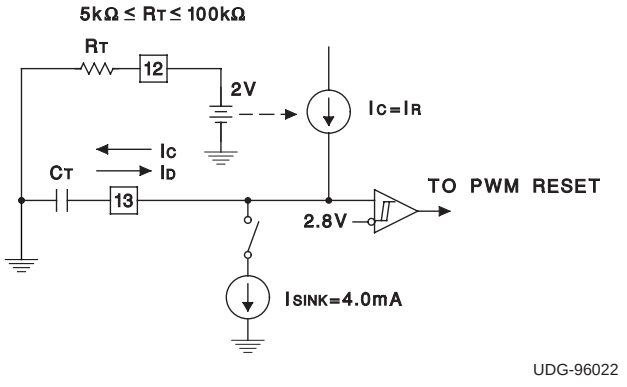


Figure 1. Oscillator

Configuring the Current Sense Amplifier

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, R_{SENSE}. This amplifier must be set up as a differential amplifier as shown.

The Current Sense Amplifier gain, G_{CSA}, is given by the ratio of R2/R1. The output of the Current Sense Amplifier at the ISO pin is given by

$$V_{ISO} = V_{BUF} + V_{SENSE} \bullet \frac{R2}{R1}$$

The Current Sense Amplifier gain, G_{CSA}, must be programmed to be greater than or equal to 5.0 (14dB), as this amplifier is not stable with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore G_{CSA} must be programmed between

$G_{CSA_MIN} = 5.0$ and $G_{CSA_MAX} = 2.5MHz/F_{SWITCH}$

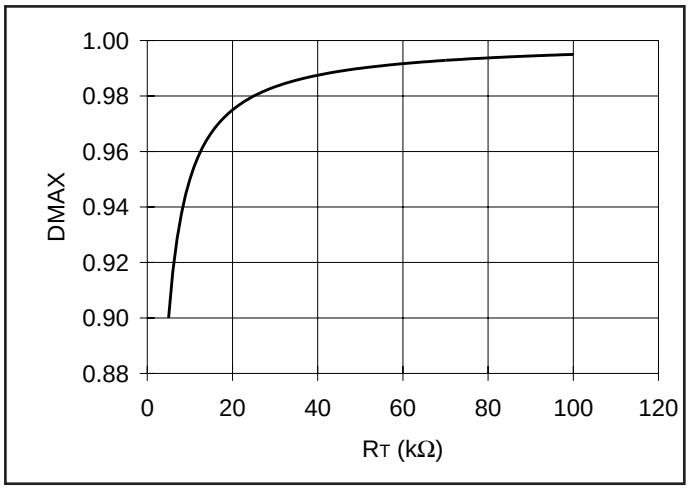


Figure 2. Programming Maximum Duty Cycle with RT

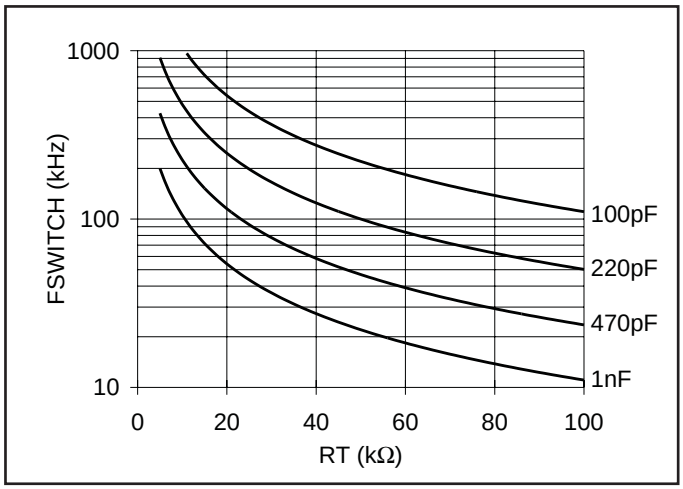


Figure 3. Programming Switching Frequency with CT

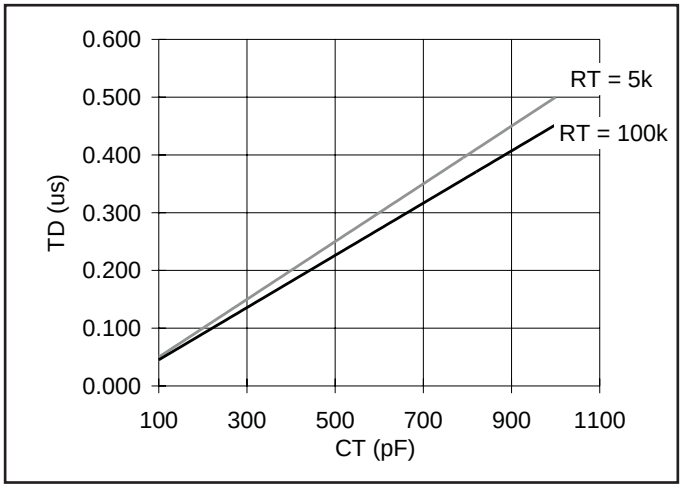


Figure 4. Deadtime vs. CT and RT

APPLICATION INFORMATION (cont.)

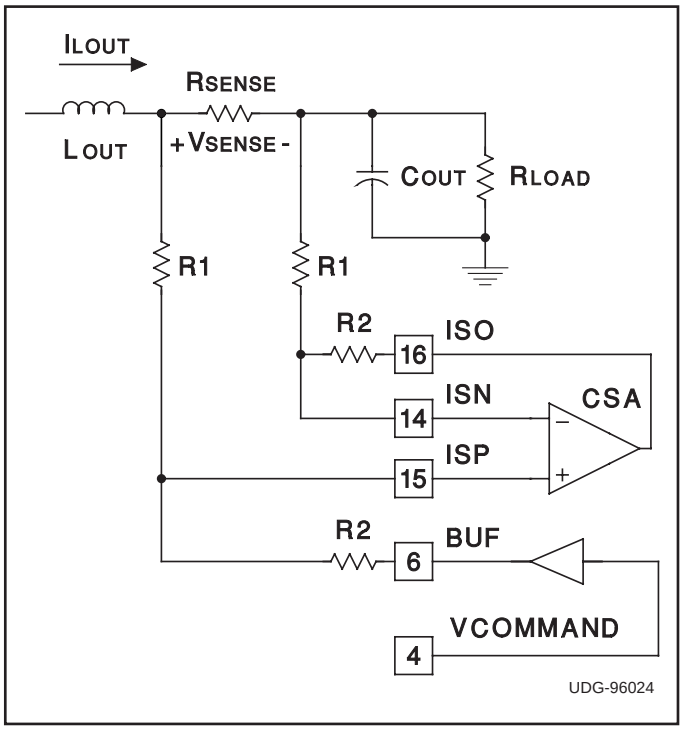


Figure 5. Configuring the Current Sense Amplifier

Enabling/Disabling the UC3886 Gate Drive

The CAO/ENBL pin can be used to Disable the UC3886 gate drive by forcing this pin below 0.8V, as shown. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effectively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.

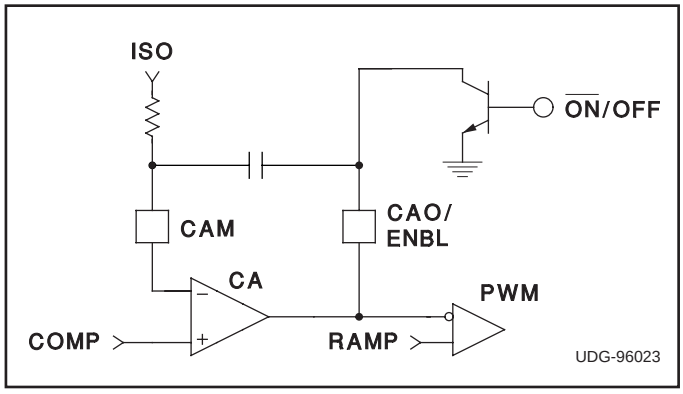


Figure 6. Enabling/Disabling the UC3886

TYPICAL APPLICATIONS

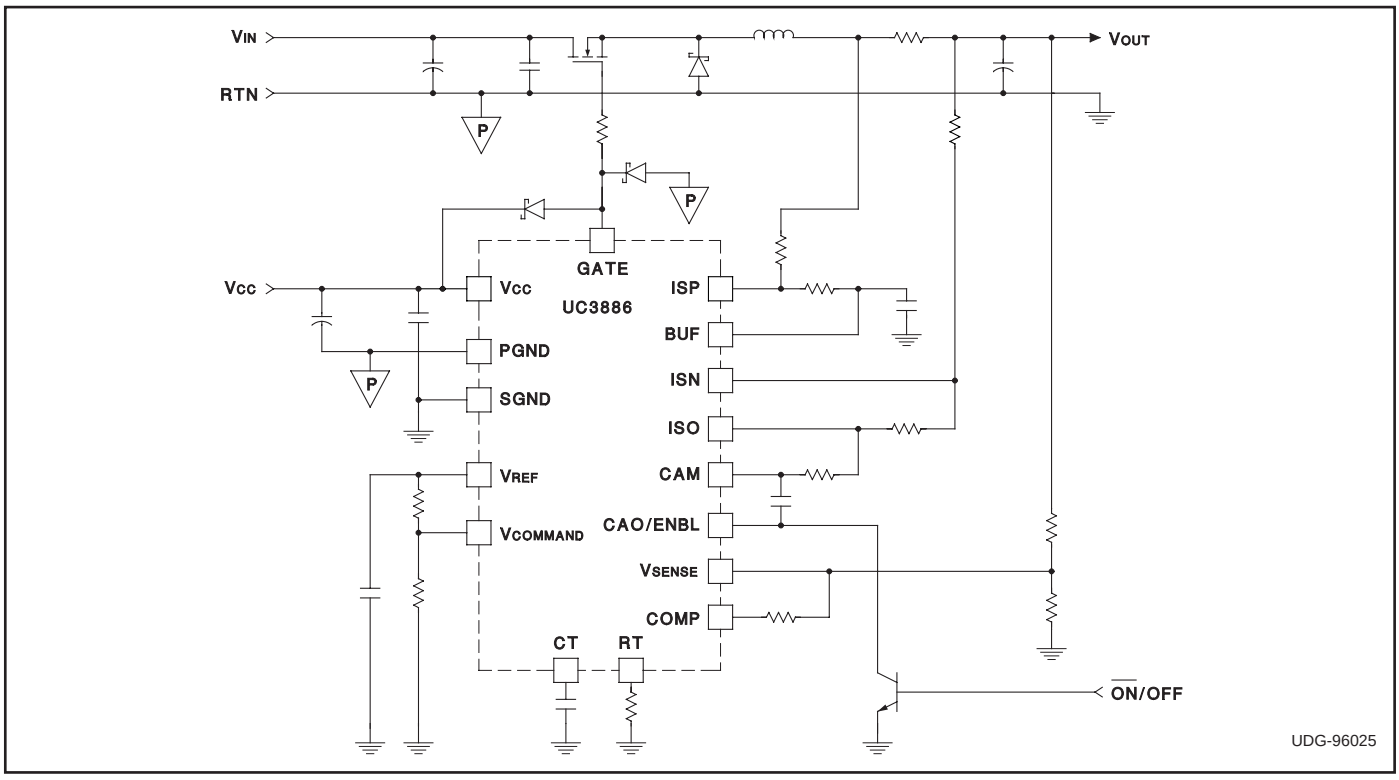


Figure 7. The UC3886 Configured in a Buck Regulator

TYPICAL APPLICATIONS (cont.)

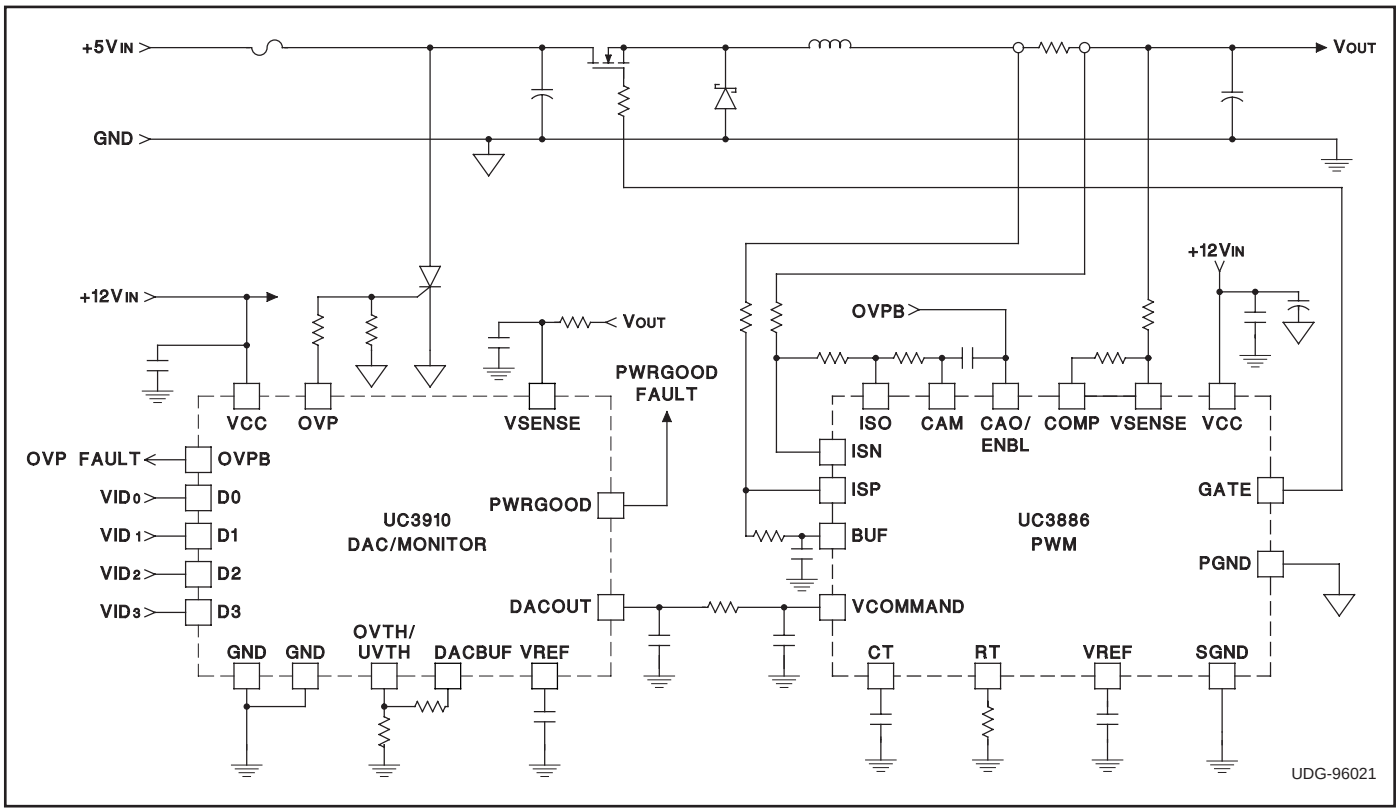


Figure 8. UC3886 Configured with the UC3910 for a Pentium® Pro DC/DC Converter

UNITRODE CORPORATION
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2886D	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2886D	
UC2886DG4	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2886D	
UC3886D	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3886D	
UC3886DG4	LIFEBUY	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3886D	
UC3886DTR	LIFEBUY	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
UC3886N	LIFEBUY	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3886N	
UC3886NG4	LIFEBUY	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3886N	

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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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